IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

U.S. ETHERNET INNOVATIONS, LLC,

Plaintiff,

v.

ACER, INC., et al.,

Defendants.

and

ATHEROS COMMUNICATIONS, INC., et al.,

Intervenors.
_____/

No. C 10-3724 CW

ORDER ON SUMMARY JUDGMENT MOTIONS

(Docket Nos. 1133 and 1167)

U.S. ETHERNET INNOVATIONS, LLC,

Plaintiff,

v.

AT&T MOBILITY, LLC, et al.,

Defendants.
_____/

No. C 10-5254 CW

ORDER ON SUMMARY JUDGMENT MOTIONS

In this consolidated patent infringement case, Plaintiff U.S. Ethernet Innovations, LLC (USEI) moves for summary judgment on a number of discrete issues: infringement of claim 21 of the '872 patent against Intel, Intel's intentional copying of the patented inventions, validity of the '872 and '094 patents in view of the SONIC prior art reference, and Defendants' claims of inequitable

conduct.[1] Defendants and Intervenors (collectively, Defendants) oppose the motion and affirmatively move for summary judgment on the issues of damages, non-infringement of the '313 patent, anticipation of certain claims of the '872 and '094 patents by the Intel 82593 prior art reference, anticipation of all asserted claims of the '872 and '094 patents by the SONIC prior art reference, non-infringement of the '459 patent, invalidity of certain '313 and '459 patent claims under § 112, and issues specific to AT&T Services (ATTS), Marvell (MSI), Apple, and Atheros/Sigma/ATTS. The motions were heard on August 14, 2014. Having considered the parties' submissions and the arguments of counsel, the Court grants some motions and denies others, and grants some motions in part.

BACKGROUND

3Com Corporation, USEI's predecessor-in-interest, developed ethernet technology in the 1980s and 1990s. In the early 1990s, 3Com obtained the four patents-in-suit: U.S. Patent Nos. 5,434,872 (the '872 patent) (Apparatus for automatic initiation of data transmission), 5,732,094 (the '094 patent) (Method for automatic initiation of data transmission), 5,307,459 (the '459 patent) (Network adapter with host indication optimization), and 5,299,313 (the '313 patent) (Network interface with host independent buffer management).

[1] Defendants have withdrawn their inequitable conduct claims. Thus, the Court need not address this issue.

The patents-in-suit relate to the field of network interface controllers/adapters for managing the transmission and reception of data between a host computer system and a communication network. '313 patent, Field of the Invention. Typically, these controllers manage the transfer of data between the host computer system and the communication network, relieving the host computer to perform other tasks. Id., Description of Related Art. Using such a network controller, a sender may transmit "packets" or "frames" of data across a communication network. '872 patent, Description of Related Art. The frames of data must be organized according to the network "protocol" before transmission. Id. Some network adapters include dedicated transmit buffers, which can download data of a frame before they are transmitted. Id. A dedicated transmit buffer allows the host computer system to attend to other tasks while the data frame is being processed and transmitted. Id. If frame transmission is cancelled, the data may be retained in the transmit data buffer until the sending system tries to transmit the frame again. Id.

On October 9, 2009, USEI filed suit in the Eastern District of Texas against sixteen computer maker defendants,[2] alleging that they were manufacturing and selling desktop and laptop computers

[2] Acer, Inc., Acer America Corporation, Apple, Inc., ASUS Computer International, Asustek Computer, Inc., AT&T Services, Inc., Dell, Inc., Fujitsu Ltd., Fujitsu America, Inc., Gateway, Inc., Hewlett Packard Co., Sony Corporation, Sony Corporation of America, Sony Electronics, Inc., Toshiba Corporation, Toshiba America, Inc., and Toshiba America Information Systems, Inc.

which incorporated chips supplied by others that practice certain ethernet technology, thereby infringing the four patents-in-suit. That case was subsequently transferred to this district and given Case No. 10-3724 (the Acer case). On March 10, 2010, USEI filed a separate suit in the Eastern District of Texas against the retailer Defendants,[3] alleging infringement of the same four patents-in-suit. That case was subsequently transferred to this district and given Case No. C 10-5254 (the AT&T case). Chip suppliers, including Intel, Marvell, Atheros, and Sigma, who designed and provided chips to Defendants, successfully moved to intervene in both cases. The cases against the retailer Defendants and ATTS were stayed.

The Court has issued two claim construction orders. See Case No. C 10-3724, Docket Nos. 586 and 634; Case No. C 10-5254, Docket Nos. 331 and 379.

LEGAL STANDARDS

Summary judgment is appropriate only where the moving party demonstrates there is no genuine dispute as to any material fact such that judgment as a matter of law is warranted. Fed. R. Civ. P. 56(a); Celotex Corp. v. Catrett, 477 U.S. 317, 323 (1986). Material facts are those that might affect the outcome of the case, as defined by the framework of the underlying substantive

[3] AT&T, Inc., Barnes & Noble, Inc., Claire's Stores, Inc., J.C. Penney Company, Inc., Sally Beauty Holdings, Inc., and Home Depot U.S.A., Inc.

law. Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 248 (1986). A dispute is genuine if the evidence is such that a reasonable jury could return a verdict for either party. Id.

The moving party bears the initial burden of informing the district court of the basis for its motion and identifying those portions of the pleadings, discovery, and affidavits that demonstrate the absence of a disputed issue of material fact. Celotex, 477 U.S. at 323. In opposing the motion, the non-moving party may not rely merely on the allegations or denials in its pleadings, but must set forth "specific facts showing that there is a genuine issue for trial." Anderson, 477 U.S. at 248 (citing Fed. R. Civ. P. 56(e)). The court must construe the evidence in the light most favorable to the non-moving party, making all reasonable inferences that can be drawn. Matsushita Elec. Indus. Co., Ltd. v. Zenith Radio Corp., 475 U.S. 574, 587 (1986); Intel Corp. v. Hartford Accident & Indem. Co., 952 F.2d 1551, 1558 (9th Cir. 1991); Eisenberg v. Ins. Co. of N. Am., 815 F.2d 1285, 1289 (9th Cir. 1987).

DISCUSSION

I. Anticipation of the asserted claims of the '872 and '094 patent by the SONIC prior art reference

A. USEI's motion

USEI moves for summary adjudication that the SONIC reference cannot anticipate the '872 and '094 patents (the "Early Transmit" patents), because it lacks a buffer memory of a certain minimum

size as required by the balance of the claim language. Defendants disagree, and cross-move for summary judgment that the asserted claims are anticipated by the SONIC prior art.

Patents are presumed valid, and the presumption may only be overcome by clear and convincing evidence. Microsoft Corp. v. i4i Ltd. P'ship, 131 S. Ct. 2238, 2252 (2011). "The burden of establishing invalidity of a patent . . . shall rest on the party asserting such invalidity." 35 U.S.C. § 282(a). Title 35 U.S.C. § 102 establishes the various grounds for invalidation of patents based on anticipation by prior art. "Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim." Therasense, Inc. v. Becton, Dickinson and Co., 593 F.3d 1325, 1333 (Fed. Cir. 2010) (quoting Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

There is no dispute that SONIC is prior art pursuant to 35 U.S.C. § 102. SONIC is referred to in the Description of Related Art sections of the '872 and '094 patents as "representative prior art." There is also no dispute that the SONIC device contains a thirty-two byte buffer memory, not big enough to hold the smallest ethernet data frame, which is sixty-four bytes in size.

USEI contends that the plain language of the '872 and '094 patents demonstrates that the buffer memory must be big enough to hold an entire ethernet frame. For example, USEI points to claim 1 of the '872 patent, which calls for: "initiating transmission of

the frame prior to transfer of all the data of the frame to the buffer memory from the host computer." USEI then points to claim 21, which requires "logic which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame from the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory." USEI finally refers to the Court's construction of "buffer memory" as "memory for the temporary storage of data" to argue that, taken as a whole, the buffer memory of the patented invention must be capable of holding a complete minimum-sized ethernet data frame from the host computer "all at one time."

USEI's argument is unpersuasive. First, the plain language of the claims says nothing about the buffer memory's ability to hold a complete frame of data. Instead, it states more or less the opposite -- that a complete frame need not be downloaded into buffer memory before transmission can occur. The claim language USEI points out supports only the notion that a complete download of a frame need not occur. In other words, the language does not require that the buffer memory have the capacity to store all of the data of a frame at once, only that the transmission of the frame away from the buffer memory is initiated before all of the data of the frame is fully transferred to the buffer memory. USEI's own evidence of the specification, noting the disadvantages of prior art using a dedicated transmit buffer that accommodated a

full data frame, actually undermines USEI's contention; if the specification criticized the use of full frame capacity, that would indicate that the invention itself did not require full frame capacity.

Moreover, the Court construed the term "buffer memory" to mean "a memory for temporary storage of data" and did not impose any extraneous storage requirements on buffer memory. USEI previously made a similar argument that "the buffer memory is able to retain a frame of data that has been transmitted." The Court rejected this argument, finding that such additional language would add a limitation that is not required by the specification. Docket No. 586 at 21. Similarly, USEI's present attempt to infer a size requirement is simply not justified by the claim language, the specification, or any other evidence.

USEI does not present any evidence to support a finding that SONIC does not anticipate the '872 and '094 patents. Therefore, summary judgment for USEI on this point is not warranted. Instead, as will be discussed below, summary adjudication of the issue is granted for Defendants.

B. Defendants' cross motion

Because Defendants also move affirmatively that SONIC anticipates the asserted claims of the '872 and '094 patents, the Court turns to the other arguments they advance, all of which they must prove by clear and convincing evidence in order to prevail. Microsoft Corp., 131 S. Ct. at 2252-53.

To show anticipation, Defendants refer to Dr. Wicker's report, which provides invalidity analysis and invalidity claim charts that detail element-by-element how SONIC satisfies each and every asserted claim limitation in the '872 and '094 patents. See Constant Decl. Ex. 14, Wicker Rpt. at ¶¶ 554-675, Exhs 9, 11. This evidence is largely unrefuted by USEI. USEI instead pins its substantive defense on its contention that the balance of the claim language imposes a lower limit on the buffer memory capacity -- that the buffer memory, as claimed, must be large enough to hold a full-size ethernet data frame, which has a minimum size of sixty-four bytes; SONIC's thirty-two byte buffer memory cannot satisfy the "buffer memory" limitation as claimed. In essence, USEI does not dispute any relevant facts regarding the alleged anticipating SONIC prior art, but only disagrees over an interpretation of the claim language. This renders the anticipation issue one of claim construction, which is a question of law. Markman v. Westview Instruments, Inc., 517 U.S. 370, 384 (1996).

After reviewing the claim language and the specification, the Court finds no justification to require that the "buffer memory" of the "Early Transmit" patents be capable of holding of a complete minimum-sized ethernet data frame all at one time. As the Court detailed above, the plain language of the claims says nothing about the buffer memory's ability to hold a complete frame of data. Instead, it states that a complete frame need not be

downloaded into buffer memory before transmission can occur. Nothing in the specification contradicts this understanding. Accordingly, the Court grants Defendants' motion for summary adjudication that SONIC anticipates the asserted claims of the '872 and '094 patents. Because the Court finds that the asserted claims of the '872 patent are invalid due to anticipation by the SONIC prior art, the Court need not decide USEI's motion for summary judgment of infringement of claim 21 of the '872 patent.

II. Whether Intel intentionally copied the patented invention, precluding any equitable defense

USEI contends that ample evidence exists to show that Intel copied the patented technology, which should prevent Intel from asserting any equitable defense. See, e.g., A.C. Aukerman Co. v. R.L. Chaides Constr. Co., 960 F.2d 1020, 1033 (Fed. Cir. 1992) ("A patentee may also defeat a laches defense if the infringer 'has engaged in particularly egregious conduct which would change the equities significantly in plaintiff's favor.' Conscious copying may be such a factor weighing against the defendant.") USEI presents evidence that Intel began testing and discussing 3Com's ethernet technology in 1992. For example, USEI has proffered internal Intel emails discussing the value of these accused infringing technologies and how they might be implemented in upcoming products. See Nation Decl. Exs. E., F.

Intel disagrees, arguing that USEI's allegations concern the copying of a 3Com product (the Etherlink III) that USEI's own

experts could not even identify or describe, much less compare to the asserted claims. Further, Intel contends that USEI's experts never compared the asserted claims to the Intel product (the 82595TX) that was alleged to be the result of Intel's intentional copying.

In order to establish that Intel intentionally copied the patented inventions, USEI must first show that the product allegedly copied by Intel embodied the asserted claims. Without such a showing, the allegations of copying are irrelevant. See, e.g., Amazon.com, Inc. v. Barnesandnoble.com, Inc., 239 F.3d 1343, 1366 (Fed. Cir. 2001) ("[E]vidence of copying Amazon's '1-Click' feature is legally irrelevant unless the '1-click' feature is shown to be an embodiment of the claims.").

The proffered internal Intel emails refer to "Parallel Tasking," a 3Com marketing term describing a commercial product (the "EtherLink III" adapter) that 3Com released in 1992. USEI fails to provide any evidence to show that the "Parallel Tasking" EtherLink III adapter embodies each and every element of the asserted claims or practices them. USEI's experts admit that they have not looked into whether the EtherLink III practiced any of the asserted claims. See Constant Decl. Ex. 6, Mitzenmacher Depo. at 290:16-293:19; Ex. 10, Conte Depo. at 79:1-24. Without such a showing, to the extent that USEI's motion asserts intentional copying, it must be denied. USEI also contends, in this motion, that Defendants, including Intel, engaged in litigation misconduct

by paying critical fact witnesses to prevent them from speaking to USEI. The Court has already denied sanctions regarding these actions and addressed accessibility concerns regarding this witness. Docket Nos. 866, 900. Thus USEI's request to bar Intel from asserting any equitable defense is denied.

III. Non-infringement of the '313 patent by any of the accused products

Claims 1 and 13 are the only asserted independent claims of the '313 patent. Defendants move for summary adjudication that no accused product infringes claim 1 of the '313 patent because (1) none of the accused products practices "network interface means"; (2) none of the accused products satisfies the requirement of "buffer memory outside of the host address space;" and (3) none of the accused products practices "host interface means." Defendants further contend that no accused product infringes claim 13 because USEI failed to identify any accused product that includes the structures identified by the Court as corresponding to the "host interface means" or the "network interface means" limitation.

A. "Network interface means" in claim 1

Claim 1 of the '313 patent reads:

> An apparatus for controlling communication between a host system and a network transceiver coupled with a network, wherein the host system includes a host address space, comprising:
>
> a buffer memory outside of the host address space;

> host interface means, sharing the host address space with the host, for managing data transfers between the host address space and the buffer memory in operations transparent to the host system; and
>
> network interface means, coupled with the network transceiver, for managing data transfers between the buffer memory and the network transceiver.

Defendants contend that none of the accused products practices "network interface means" as construed by the Court.

Claim 1 of the '313 patent recites "network interface means, coupled with the network transceiver, for managing data transfers between the buffer memory and the network transceiver." The Court found that "network interface means" is a means-plus-function term governed by § 112 ¶ 6. First Claim Construction Order, Docket No. 586 at 12. The Court construed "network interface means" to perform the function of "managing data transfers between the buffer memory and the network transceiver" and the corresponding structures to be "in Figure 3, Network interface logic 104, and equivalents." Second Claim Construction Order, Docket No. 634 at 17. Figure 3 of the '313 patent shows that the "network interface logic 104" is made up of "XMIT DMA LOGIC 109" and "RECEIVE DMA LOGIC 110." The Court elaborated on its construction by pointing to the specification, which states the "network interface logic 104 includes the transmit DMA logic 109 responsive to descriptors stored in the adaptor memory 103, for moving data out of the adapter memory to the network transceiver 105." Id.; '313 Patent, 10:3-11.

Defendants contend that the accused infringing products do not "transmit DMA logic responsive to descriptors stored in the adaptor memory" because all accused products move data from the buffer memory onto the network irresponsive to transmit descriptors stored in adapter memory. Kunz Decl. at ¶¶ 19-23; Carkin Decl. at ¶ 7; McCauley Decl. Ex. 1, Lin Rpt. at ¶¶ 156-169; Hu Decl. Ex. 1, Lin Rpt. for Sigma at ¶¶ 81-91, 152-162. USEI responds that, to prove infringement under the Court's construction, all it needs is to identify a "network interface logic 104" that performs the function of "managing transfers of data from buffers in the independent memory 103 and the network transceiver 105"; it does not need to identify further the corresponding structure to "transmit DMA logic 109 responsive to descriptors stored in adapter memory for moving data out of the adapter memory to the network transceiver."

Thus, the debate hinges on what is required to show infringement of "network interface means," a term the Court found to be governed by § 112 ¶ 6. Literal infringement of a claim limitation governed by § 112 ¶ 6 requires that the relevant structure in the accused device (1) perform the identical function recited in the claim, and (2) be identical or equivalent to the corresponding structure in the specification. See Applied Med. Resources Corp. v. United States Surgical Corp., 448 F.3d 1324, 1333 (Fed. Cir. 2006). Defendants do not dispute that the identified structures in the accused products perform the

identical function of "managing data transfers between the buffer memory and the network transceiver." Defendants also do not dispute that the corresponding structure in the specification is the network interface logic 104 shown in Fig. 3, which includes transmit DMA logic 109 that is responsive to descriptors stored in the adapter memory for moving data out of the adapter memory to the network transceiver. In fact, Dr. Mitzenmacher confirmed that the Court's construction requires just such logic. Constant Decl. Ex. 6, Mitzenmacher Depo. at 163:21-164:13. Instead, the parties dispute whether the identified structures in the accused products are identical or equivalent to the corresponding structure in the specification. In this regard, Dr. Mitzenmacher fails to proffer any evidence that the identified structures in the accused products are identical or equivalent to the corresponding structure identified by the Court. For example, in his initial Intel Report, Dr. Mitzenmacher identifies the MAC core component in Intel Gigabit products as the "network interface means" but fails to identify any DMA logic that is "responsive to descriptors stored in the adapter memory for moving data out of the adapter memory to the network transceiver." Constant Decl. Ex. 7, Mitzenmacher Intel Rpt. at ¶ 239. In fact, Dr. Mitzenmacher concedes that he did not specifically identify any such DMA logic in the MAC core component. Nation Decl. Ex. 41, Mitzenmacher 5/30 Depo. at 377:20-381:3. Likewise, Dr. Mitzenmacher's report for MSI makes no mention of any structure in the accused products that

is "responsive to descriptors stored in adapter memory for moving data out of adapter memory to a network transceiver." Flynn-O'Brien Decl. Ex. 6, Mitzenmacher Marvell Rpt. at ¶ 69, Ex. 8, Mitzenmacher Depo. at 626:12-22. As an alternative, USEI refers to Dr. Mitzenmacher's Supplemental Reports on how the structures identified in his initial reports are equivalent to the "transmit DMA logic 109 that is responsive to descriptors stored in the adapter memory for moving data out of the adapter memory to the network transceiver." However, the Court has not allowed these supplemental reports. As a result, USEI is foreclosed from arguing that the structures identified in Dr. Mitzenmacher's initial reports are equivalent to the "transmit DMA logic 109." Accordingly, because no structure in any accused product infringes the "network interface means" limitation of claim 1 of the '313 patent, summary judgment of non-infringement by any of the accused products of claim 1 of the '313 patent is appropriate.

B. "Buffer memory outside of host address space" in claim 1

Defendants contend that USEI fails to make a showing that the limitation "a buffer memory outside of the host address space" is met because the identified buffer memory in the accused Intel products can be accessed by the host under some circumstances, which implies that the buffer memory is not "outside of the host address space."

In his infringement report against Intel, Dr. Mitzenmacher identifies first-in-first-out buffers (FIFOs) in the accused Intel

products as the alleged "buffer memory outside of the host address space" recited in claim 1. Constant Decl. Ex. 7, Mitzenmacher Intel Rpt. at ¶ 230. However, Dr. Mitzenmacher concedes that "the Intel technical documentation for at least some of these products allows for direct addressing to the data FIFO buffers by the host specifically for diagnostic purposes." Id. at ¶ 231. These FIFOs in the accused Intel products do not meet the "buffer memory outside of the host address space" requirement because they are accessible by the host system and, thus, lie within the host address space. USEI contends that these FIFOs are only accessible by the host during diagnosis but are inaccessible to the host during normal data transmission, thereby rendering them "outside of the host address space" during the relevant time. Id. USEI's contention fails as a literal infringement argument; the buffer memory can either be inside or outside the host address space, but not both. To the extent that USEI argues that the FIFOs in the accused Intel products are equivalent to "buffer memory outside of the host address space," that is a doctrine of equivalents argument, one for which USEI has failed to proffer any evidence. Therefore, summary judgment of non-infringement of claim 1 of the '313 patent by the accused Intel products is appropriate for this reason as well.

Defendants further contend that Dr. Mitzenmacher improperly identifies two distinctly different "buffer memories" in each accused product for different limitations in claim 1, even though

the claim only mentions one "buffer memory." For example, Dr. Mitzenmacher identifies "packet buffer data FIFO buffers" in the accused Intel products as the "buffer memory outside the host address," but identifies "transmit and receive descriptor ring buffers" as the "buffer memory" of the "host interface means." Id. at 230, 233. Similarly, for each accused MSI product, Dr. Mitzenmacher identifies the "MAC Rx and Tx FIFOs" as the "buffer memory outside of the host address space," but the combination of the "MAC Rx and Tx FIFOs" and the "PFU Rx and Tx FIFOs" as the "buffer memory" of the "host interface means." Flynn-O'Brien Decl. Ex. 6, Mitzenmacher Marvell Rpt. at ¶¶ 61-67. USEI does not dispute this showing, but instead argues that this is covered by claim 1.

Claim 1 only recites one buffer memory in the "host interface means," which is for "managing data transfers between the host address space and the buffer memory," a reference to the "buffer memory outside of the host address space." Therefore, to show literal infringement, USEI must identify one "buffer memory" that performs the claim function. To the extent that USEI argues that the two identified buffer memories are equivalent to "the buffer memory" recited in the claim, that requires a showing of equivalency, for which USEI has failed to proffer any evidence. Therefore, summary judgment of non-infringement of claim 1 of the '313 patent by the accused Intel and MSI products is appropriate for this reason as well.

C. "Host interface means" in claim 1

Claim 1 contains the limitation of "host interface means," which the Court construed as having the function of "managing data transfer between address spaces on the host system bus and the buffer memory in operations performed independently of management by the host system." First Claim Construction Order, Docket No. 586 at 10-11. Defendants contend that the Court's construction that the data transfer must be "performed independently of management by the host system" dictates that the host system cannot be involved in data transfers. As a result, Defendants argue no infringement can be shown because the host systems in all accused products are involved in managing the data transfers between the host system and the network adapter by writing descriptors to a queue in the host system's memory (i.e., the "host address space.") Defendants' Motion and Opposition, Docket No. 1167-3 at 17.

Because, as discussed above, the Court finds that claim 1 of the '313 patent is not infringed for other reasons, the Court need not address this issue.

D. "Host interface means" in claim 13

Defendants contend that USEI fails to apply the Court's construction of the "host interface means" in claim 13 of the '313 patent to identify the relevant structures in the accused products and, instead, improperly applies the construction from claim 1.

Claim 13 reads:

> An apparatus for controlling communication between a host system and a network transceiver coupled with a network, wherein the host system includes a host address space, comprising:
>
> a buffer memory outside of the host address space, including a transmit buffer and a receive buffer;
>
> host interface means, sharing host address space including a prespecified block of host addresses of limited size defining a first area and a second area, and coupled with the buffer memory, for mapping data addressed to the first area into the transmit buffer, mapping data in the receive buffer into the second area, and uploading data from the receive buffer to the host; and
>
> network interface means, coupled with the network transceiver and the buffer memory, for transferring data from the transmit buffer to the network transceiver and mapping data into the receive buffer from the network transceiver.

Unlike claim 1, which recites a "host interface means" that performs a single function of "managing data transfers between the host address space and the buffer memory in operations transparent to the host system," claim 13 recites three functions for the "host interface means," namely, "mapping data addressed to the first area into the transmit buffer," "mapping data in the receive buffer into the second area," and "uploading data from the receive buffer to the host." Second Claim Construction Order, Docket No. 634 at 16. The Court identified separate corresponding structures for each identified function, including an XMIT AREA register, transfer descriptor logic; an XFER AREA register, upload logic; and an upload DMA module, respectively. Id.

USEI fails to base its infringement analysis on the Court's construction for claim 13, but instead applies the construction from claim 1. See Constant Decl. Ex. 53, Mitzenmacher Intel Base Rpt. at ¶ 250. USEI contends that Dr. Mitzenmacher's reports identify structures in the accused products that perform the functions recited by the Court for the "host interface means" element of the '313 patent. Nation Decl. Ex. 35, Mitzenmacher 5/29 Depo. at 168:6-172:14, 175:8-21. However, the record does not support USEI's contention. Claim 13 clearly recites three functions for "host interface means" but USEI fails specifically to identify structures in the accused device that perform these functions. Literal infringement of a claim limitation governed by § 112 ¶ 6 requires that the relevant structure in the accused device (1) perform the identical function recited in the claim, and (2) be identical or equivalent to the corresponding structure in the specification. Applied Med. Resources, 448 F.3d at 1333. USEI fails to show even the first requirement that the relevant structure in the accused device perform the identical function recited in the claim, let alone the second requirement that the relevant structures be identical or equivalent to the corresponding structures. Therefore, USEI fails to show an issue of fact regarding infringement of claim 13 of the '313 patent and, thus, summary judgment of non-infringement of that claim by any of the accused products is warranted.

IV. Anticipation of claim 21 of the '872 patent and claims 9, 28, and 39 of the '094 patent by the Intel 82593 prior art reference

Defendants move for partial summary adjudication of anticipation under 35 U.S.C. § 102(a) and (b), contending that Intel's 82593 chip is prior art that satisfies every limitation of claim 21 of the '872 patent and claims 9, 28, 39 of the '094 patent. However, as discussed above, the Court grants summary adjudication of invalidity of all the asserted claims of the '872 and '094 patents due to the SONIC prior art reference. Thus, the Court need not address this issue.

V. Non-infringement of the '459 patent by any of the accused products

Claims 1 and 44 are the only asserted independent claims of the '459 patent, and they are asserted only against Intel (claim 1) and HP (claims 1 and 44).

A. "Means for comparing"

Defendants contend that USEI's infringement reports regarding Intel and HP fail to establish infringement because they ignore that the "means for comparing" recited in the claims is a means-plus-function element governed by § 112 ¶ 6 and do not address any of the corresponding structures in the '459 patent that the Court identified for such means (e.g., blocks 224 and 318, interrupt controller 60), much less show that such structures are satisfied by the accused Intel or HP products. Constant Decl. Ex. 12, Crayford Rpt. at ¶¶ 859-861.

As noted above, literal infringement of a claim limitation governed by § 112 ¶ 6 requires that the relevant structure in the accused device (1) perform the identical function recited in the claim, and (2) be identical or equivalent to the corresponding structure in the specification. Applied Med., 448 F.3d at 1333.

Claim 1 of the '459 patent reads:

> An apparatus for transferring a data frame between a network transceiver, coupled with a network, and a host system which includes a host processor and host memory, the apparatus generating an indication signal to the host processor responsive to the transfer of the data frame, with the host processor responding to the indication signal after a period of time, comprising:
>
> a buffer memory for storing the data frame;
>
> network interface logic for transferring the data frame between the network transceiver and the buffer memory;
>
> host interface logic for transferring the data frame between the host system and the buffer memory;
>
> threshold logic for allowing the period of time for the host processor to respond to the indication signal to occur during the transferring of the data frame, wherein the threshold logic includes,
>
> > a counter, coupled to the buffer memory, for counting the amount of data transferred to or from the buffer memory;
> >
> > an alterable storage location containing a threshold value; and
> >
> > means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location.

Claim 44 contains more or less the same language for "means for comparing."

The Court construed "means for comparing" to have two functions: (1) "comparing the counter to the threshold value in the alterable storage location"; and (2) "generating an indication signal to the host processor." The Court found that the block labeled 224 in Fig. 14 and 318 in Fig. 21 performs the first function. Second Claim Construction Order, Docket No. 634 at 10-11. The Court found that the functional components labeled "Interrupt Controller 60" shown in Fig. 4, together with "Early Rcv Control 225" in Fig. 14, perform the second function. Id.

USEI argues that Dr. Mitzenmacher "identifies structures performing the required functions taking into account the Court's claim construction in his original Infringement Reports," but his report merely identifies a portion of the Intel source code of the accused products performing the comparison function without identifying any structure corresponding to the structures specified in the Court's construction. Constant Decl. Ex. 7, Mitzenmacher Intel Rpt. at ¶ 210; Constant Decl. Ex. 12, Crayford Rpt. at ¶¶ 859-61. Similarly, for the accused HP products, Dr. Mitzenmacher simply opines that the recited function is performed, without regard to the corresponding structure required by the Court's claim construction. Declaration of Cameron A. Zinsli (Zinsli Decl.), Ex. 2, Mitzenmacher HP Rpt. at ¶¶ 119, 120. This is not sufficient; USEI must identify structures in the accused product that are either identical or equivalent to the corresponding structures identified by the Court. Applied Med.,

448 F.3d at 1333. As an alternative, USEI points to Dr. Mitzenmacher's Supplemental Reports for evidence that the proffered source code is at least equivalent to that required by the Court. However, these reports have been excluded. Therefore, USEI is foreclosed from arguing that the identified source code is equivalent to the corresponding structures required by the Court. Accordingly, summary judgment of non-infringement of claims 1 and 44 of the '459 patent by the accused Intel and HP products is granted.

B. "Look-ahead threshold logic"

Intel separately contends that claim 1 of the '459 is not infringed because Intel's accused products do not satisfy "means for comparing" in that they do not contain the "look-ahead threshold logic" required by the Court's construction. However, as discussed above, given that summary adjudication of non-infringement of claims 1 and 44 of the '459 patent by the accused Intel and HP products is granted, the Court need not address whether Intel's products do not infringe claim 1 for this additional reason.

C. "Threshold value"

In addition, Defendants contend that claims 1 and 44 of the '459 patent are not infringed because the accused products do not satisfy "an alterable storage location containing a threshold value" limitation in claim 1 and "an alterable storage location containing a transfer threshold value" limitation in claim 44.

Again, as discussed above, given that summary adjudication of non-infringement of claims 1 and 44 of the '459 patent by the accused Intel and HP products is granted for other reasons, the Court need not decide this issue.

VI. Invalidity under § 112 of claim 13 of the '313 patent and claim 1 of the '459 patent

Defendants contend that nothing in the '313 or '459 patents suggests a single structure for performing the functions recited for the "host interface means" of claim 13 of the '313 patent and the "means for comparing" of claim 1 of the '459 patent, and ask the Court to invalidate the claims as indefinite under 35 U.S.C. § 112. However, as discussed above, the Court grants summary adjudication of non-infringement of claim 13 of the '313 patent and claim 1 of the '459 patent. Thus, the Court need not decide this issue.

VII. Exclusion of the unreliable opinion of USEI's damages expert, Walter Bratic

Defendants contend that USEI cannot prove damages, because its expert, Mr. Bratic, used unreliable methods, unreasonable inferences and speculation to reach his damages conclusions and, thus, his testimony should be excluded.

However, given the findings in this order, this motion is moot, and the Court need not address it.

VIII. ATTS' motion for partial summary judgment of no damages or, alternatively, to limit the AT&T royalty base

ATTS moved for summary judgment to limit the AT&T royalty base to the number of Sigma chips purchased during the relevant

time period. Given the other findings in this order, this motion is moot, and the Court need not address it.

IX. MSI's motion for partial summary judgment to exclude foreign non-party sales from USEI's asserted damages base

MSI contends that the damages USEI claims against it are improper in that they include Yukon chips that are manufactured abroad by third-party foundries or offered for sale and sold abroad by non-party Marvell Asia Pte. Ltd. (MAPL), a Singapore corporation that is a legal entity distinct from MSI. Declaration of Joseph Kuo (Kuo Decl.) at ¶¶ 9, 10. However, given the other findings in this order, the Court need not address this issue.

X. Apple's motion for partial summary judgment of non-infringement of claims 1, 9, 12 and 28 of the '094 patent

USEI accuses certain Apple products of infringing method claims 1, 9, 12, and 28 of the '094 patent based solely on its inclusion of GEM ethernet technology supplied by Sun Microsystems. Declaration of Christopher Cravey (Cravey Decl.) Ex. 1, Mitzenmacher Apple Rpt. at ¶¶ 52-84. Apple contends that it does not infringe these method claims because it has always disabled the accused infringing "Early Transmit" feature in the Sun GEM ethernet technology, thus rendering use of the accused infringing feature impossible. Cravey Decl. Ex. 3, Seifert Rpt. at ¶¶ 48-52, 54-57, and 64-69.

Because the Court grants summary adjudication of invalidity of all the asserted claims of the '094 patent due to the SONIC prior art reference, the Court need not address this issue.

XI. Atheros, Sigma and ATTS's motion for partial summary judgment of non-infringement of the '313 patent

In construing the '313 patent's claim 1 element, "host interface means," the Court found that the function of "managing data transfers between the host address space and the buffer memory in operations transparent to the host system" necessarily includes the function of remapping a section of the host address space in the host system to the buffer memory. Second Claim Construction Order, Docket No. 634 at 13. Atheros, Sigma and ATTS contend that Dr. Mitzenmacher's report does not provide any analysis to indicate that these Defendants' accused products practice the claims under the Court's construction. Sigma and ATTS argue that the same is true for the claims dependent on claim 1 in the '313 patent, as well as claim 13 and its dependent claims.

However, as discussed above, the Court grants summary adjudication of non-infringement of the asserted claims of the '313 patent by any of the accused products. Thus, the Court need not address this issue.

CONCLUSION

As discussed above, the Court has adjudicated the status of each asserted claim of the patents-in-suit as follows:

The Court (1) DENIES USEI's motion for summary adjudication of non-anticipation of the asserted claims of the '872 or '094 patents by the SONIC prior art reference, and instead GRANTS

Defendants' motion for invalidity of the asserted claims of the '872 or '094 patents in view of the SONIC prior art reference; (2) DENIES USEI's motion for summary judgment against Intel, and Defendants using Intel chips, of infringement of claim 21 of the '872 patent as moot; and (3) DENIES USEI's motion for summary judgment that Intel may not present any equitable defense because it intentionally copied USEI's patented invention.

With regard to Defendants' motions for summary judgment, the Court GRANTS the following motions: (1) for summary adjudication that SONIC anticipates the asserted claims of the '872 and '094 patents; (2) for summary adjudication of non-infringement of claims 1 and 13 of the '313 patent by any of the accused products; and (3) for summary adjudication of non-infringement of claims 1 and 44 of the '459 patent by the Intel and HP accused products.

The Court DENIES the following Defendants' motions as moot: (1) to exclude Mr. Bratic's expert testimony regarding all four patents-in-suit as moot; (2) for summary adjudication of anticipation of claim 21 of the '872 patent by the Intel 82593 chip prior art; (3) for summary adjudication of anticipation of claims 9, 28 and 39 of the '094 patent by the Intel 82593 chip prior art; (4) for summary judgment of invalidity, under § 112, of claim 13 of the '313 patent and claim 1 of the '459 patent; (5) MSI's motion for partial summary judgment to exclude foreign non-party sales from USEI's asserted damages base; (6) Apple's motion for summary adjudication of non-infringement of claims 1,

9, 12 and 28 of the '094 patent; and (7) Atheros, Sigma and ATTS's motion for partial summary judgment of non-infringement of the '313 patent.

Accordingly, all of the asserted claims of the patents-in-suit are resolved in favor of Defendants. The Clerk of the Court shall enter judgment in favor of Defendants, who shall recover costs from USEI.

IT IS SO ORDERED.

Dated: November 7, 2014

CLAUDIA WILKEN
United States District Judge